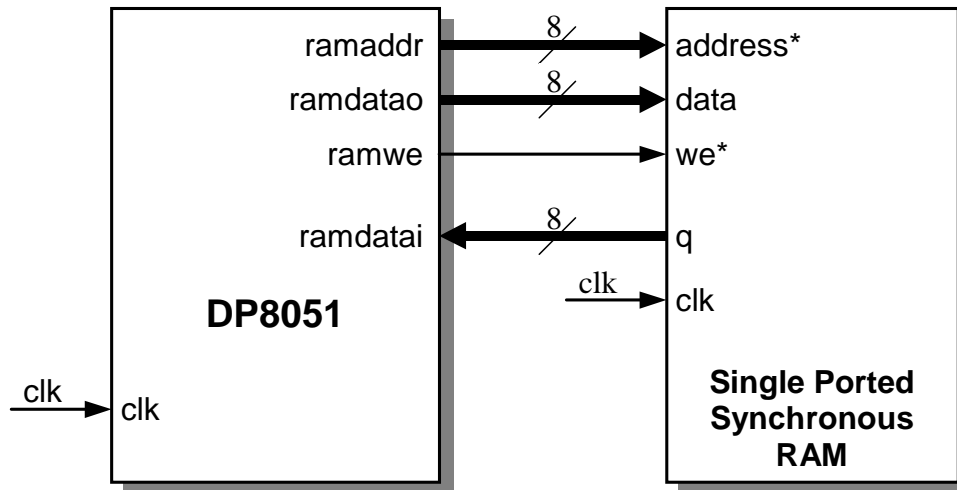


DP8051 core interfacing with Internal Synchronous Data Memory

The figure below shows the example DP8051 core interfacing with Internal Synchronous Data Memory.



* signals internally registered by clk

DP8051 core interfacing with synchronous Data Memory

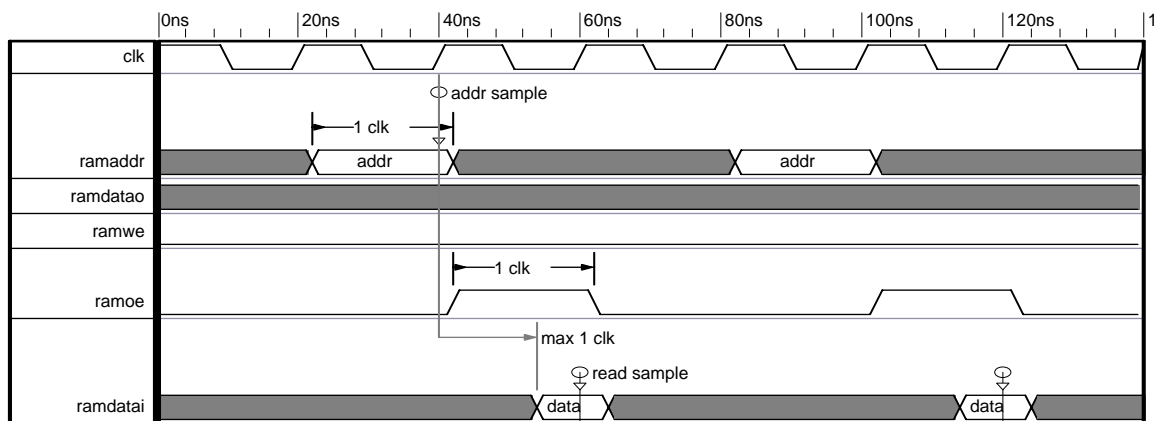


Figure 1. Internal synchronous Data Memory read cycle waveform

Note:

clk	- system clock period
ramaddr	- internal data memory address
addr	- actually read memory address
data	- data read from addr address
read sample	- data has been read from data memory and written into destination register

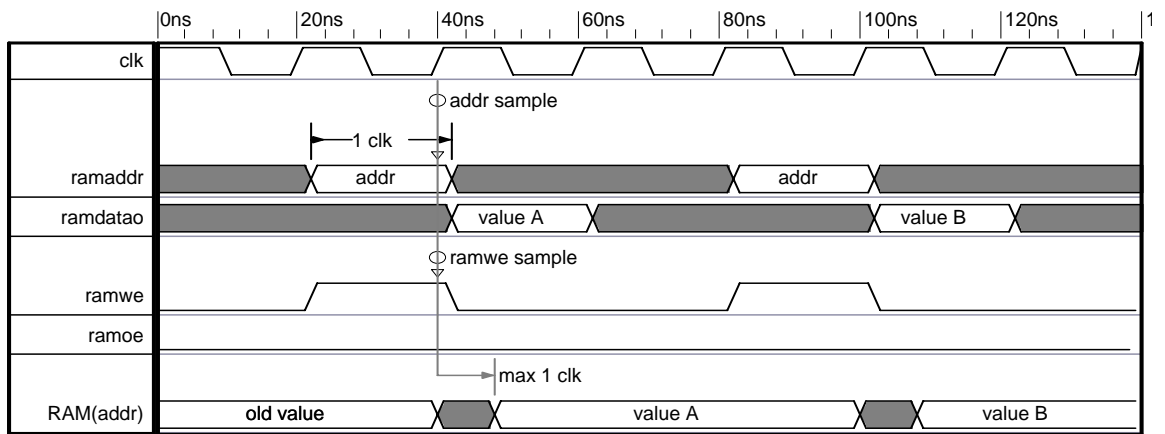


Figure 2. Internal synchronous Data Memory write cycle waveform

- Note:
- clk - system clock period
 - ramaddr - internal data memory address
 - ramwe - internal data memory write enable signal
 - value x - data written into data memory at address addr