

## DP8051 performance improvement

This document present a speed comparison of DP8051 Core vs. standard 8051 devices. In presented tables are compared numbers of CLK cycles needed to execute selected arithmetic operations. **A 1 cycle is equal to 1 CLK period.**

### a) 8-bit addition - immediate data

The following code performs immediate data (constant) addition to an 8-bit register.

$$Rx = Rx + \#n$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
<b>ADD A, #n</b>	<b>24h</b>	<b>2</b>	<b>12</b>	<b>2</b>
MOV Rx, A	F8h-FFh	1	12	1
Sum:			36	4

**DP8051 Performance Improvement: 9,0**

### b) 8-bit subtraction - direct addressing

The following code performs direct addressing subtraction from an 8-bit register.

$$Rx = Rx - (\text{dir})$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
<b>SUBB A, dir</b>	<b>25h</b>	<b>2</b>	<b>12</b>	<b>2</b>
MOV Rx, A	F8h-FFh	1	12	1
Sum:			36	4

**DP8051 Performance Improvement: 9,0**

### c) 8-bit multiplication

The following code performs the 8-bit registers multiplication.

$$Rx = Rx \cdot Ry$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
MOV B, Ry	88h-8Fh	2	24	2
<b>MUL AB</b>	<b>A4h</b>	<b>1</b>	<b>48</b>	<b>2</b>
MOV Rx, A	F8h-FFh	1	12	1
Sum:			96	6

**DP8051 Performance Improvement: 16**

**d) 8 – bit division**

The following code performs the 8-bit registers division.

$$R_x = R_x / R_y$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
MOV B, Ry	88h-8Fh	2	24	2
<b>DIV AB</b>	<b>84h</b>	<b>1</b>	<b>48</b>	<b>6</b>
MOV Rx, A	F8h-FFh	1	12	1
Sum:			96	10

**DP8051 Performance Improvement: 9,6**

**e) 16 - bit addition**

The following code performs 16-bit addition. The first operand and result are located in registers pair RaRb. Second operand is located in registers pair RxRy.

$$RaRb = RaRb + RxRy$$

Mnemonic	Opcode	Bytes	80C51 cycles	DP8051 cycles
MOV A, Rb	E8h-EFh	1	12	1
<b>ADD A, Ry</b>	<b>28h-2Fh</b>	<b>1</b>	<b>12</b>	<b>1</b>
MOV Rb, A	F8h-FFh	1	12	1
MOV A, Ra	E8h-EFh	1	12	1
<b>ADDC A, Rx</b>	<b>38h-3Fh</b>	<b>1</b>	<b>12</b>	<b>1</b>
MOV Ra, A	F8h-FFh	1	12	1
Sum:			72	6

**DP8051 Performance Improvement: 12,0**

## Performance improvement summary

Total performance improvement of DP8051 vs. standard 8051 devices has been summarized in the table below. It shows the most common used multi-precision arithmetic operation.

Function	80C51 cycle	DP8051 cycle	Improvement
8-bit addition ( <i>immediate data</i> )	36	5	<b>9,0</b>
8-bit addition ( <i>direct addressing</i> )	36	6	<b>9,0</b>
8-bit addition ( <i>indirect addressing</i> )	36	6	<b>9,0</b>
8-bit addition ( <i>register addressing</i> )	36	5	<b>12,0</b>
8-bit subtraction ( <i>immediate data</i> )	36	5	<b>9,0</b>
8-bit subtraction ( <i>direct addressing</i> )	36	6	<b>9,0</b>
8-bit subtraction ( <i>indirect addressing</i> )	36	6	<b>9,0</b>
8-bit subtraction ( <i>register addressing</i> )	36	5	<b>12,0</b>
8-bit multiplication	96	9	<b>16,0</b>
8-bit division	96	10	<b>9,6</b>
16-bit addition	72	10	<b>12,0</b>
16-bit subtraction	84	11	<b>12,0</b>
16-bit multiplication	312	32	<b>13,6</b>
32-bit addition	144	20	<b>12,0</b>
32-bit subtraction	156	21	<b>12,0</b>
32-bit multiplication	1248	142	<b>12,6</b>
<b>Average speed improvement:</b>			<b>11,12</b>