

## DR8051 performance improvement

This document present a speed comparison of DR8051 Core vs. standard 8051 devices. In presented tables are compared numbers of CLK cycles needed to execute selected arithmetic operations.

### a) immediate data

The following code performs immediate data (constant) addition to an 8-bit register.

$$Rx = Rx + \#n$$

Mnemonic	Opcode	Bytes	80C51 cycles	DR8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
<b>ADD A, #n</b>	<b>24h</b>	<b>2</b>	<b>12</b>	<b>2</b>
MOV Rx, A	F8h-FFh	1	12	2
Sum:			36	5

**DR8051 Performance Improvement: 7,2**

### b) direct addressing

The following code performs direct addressing addition to an 8-bit register.

$$Rx = Rx + (\text{dir})$$

Mnemonic	Opcode	Bytes	80C51 cycles	DR8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
<b>ADD A, dir</b>	<b>25h</b>	<b>2</b>	<b>12</b>	<b>3</b>
MOV Rx, A	F8h-FFh	1	12	2
Sum:			36	6

**DR8051 Performance Improvement: 6**

### c) indirect addressing

The following code performs indirect addressing addition to an 8-bit register.

$$Rx = Rx + (@Rx)$$

Mnemonic	Opcode	Bytes	80C51 cycles	DR8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
<b>ADD A, @Rx</b>	<b>26h-27h</b>	<b>1</b>	<b>12</b>	<b>3</b>
MOV Rx, A	F8h-FFh	1	12	2
Sum:			36	6

**DR8051 Performance Improvement: 6**

#### d) register addressing

The following code performs an 8-bit register to register addition.

$$Rx = Rx + Ry$$

Mnemonic	Opcode	Bytes	80C51 cycles	DR8051 cycles
MOV A, Rx	E8h-EFh	1	12	1
<b>ADD A, Ry</b>	<b>28h-2Fh</b>	<b>1</b>	<b>12</b>	<b>2</b>
MOV Rx, A	F8h-FFh	1	12	2
Sum:			36	5

**DR8051 Performance Improvement: 7,2**

#### e) 16 - bit addition

The following code performs 16-bit addition. The first operand and result are located in registers pair RaRb. Second operand is located in registers pair RxRy.

$$RaRb = RaRb + RxRy$$

Mnemonic	Opcode	Bytes	80C51 cycles	DR8051 cycles
MOV A, Rb	E8h-EFh	1	12	1
<b>ADD A, Ry</b>	<b>28h-2Fh</b>	<b>1</b>	<b>12</b>	<b>2</b>
MOV Rb, A	F8h-FFh	1	12	2
MOV A, Ra	E8h-EFh	1	12	1
<b>ADDC A, Rx</b>	<b>38h-3Fh</b>	<b>1</b>	<b>12</b>	<b>2</b>
MOV Ra, A	F8h-FFh	1	12	2
Sum:			72	10

**DR8051 Performance Improvement: 7,2**

## Performance improvement summary

Total performance improvement of DR8051 vs. standard 8051 devices has been summarized in the table below. It shows the most common used multi-precision arithmetic operation.

Function	80C51 cycle	DR8051 cycle	Improvement
8-bit addition ( <i>immediate data</i> )	36	5	<b>7,20</b>
8-bit addition ( <i>direct addressing</i> )	36	6	<b>6,00</b>
8-bit addition ( <i>indirect addressing</i> )	36	6	<b>6,00</b>
8-bit addition ( <i>register addressing</i> )	36	5	<b>7,20</b>
8-bit subtraction ( <i>immediate data</i> )	36	5	<b>7,20</b>
8-bit subtraction ( <i>direct addressing</i> )	36	6	<b>6,00</b>
8-bit subtraction ( <i>indirect addressing</i> )	36	6	<b>6,00</b>
8-bit subtraction ( <i>register addressing</i> )	36	5	<b>7,20</b>
8-bit multiplication	96	9	<b>10,67</b>
8-bit division	96	10	<b>9,60</b>
16-bit addition	72	10	<b>7,20</b>
16-bit subtraction	84	11	<b>7,64</b>
16-bit multiplication	312	32	<b>9,75</b>
32-bit addition	144	20	<b>7,20</b>
32-bit subtraction	156	21	<b>7,43</b>
32-bit multiplication	1248	142	<b>8,79</b>
<b>Average speed improvement:</b>			<b>7,57</b>