

Design and IP verification methodology

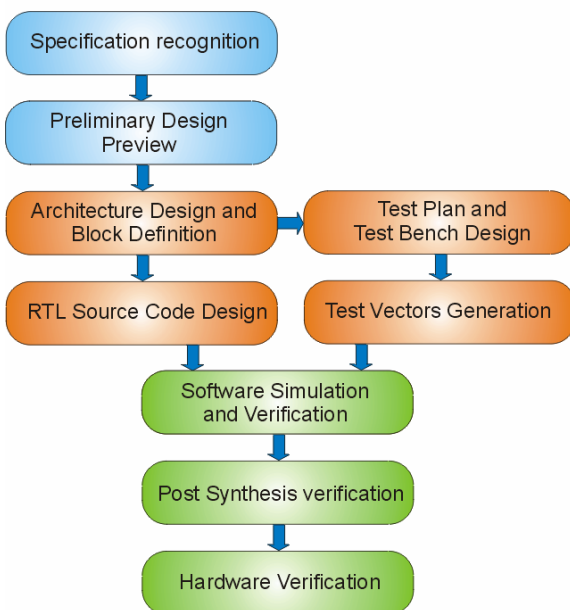
Before purchasing IP Core from third party vendor, any customer ask a question: “How well the product conform to the specification”, and “is it a bug free”?. How to proof that vendor’s IP really works and its functionality is 100% compatible with standard description? The risks may be intolerably high if it doesn’t.

There is many programs and standards which can help customer to make an objective assessment of the core quality. DCD in its design methodology and internal software development regulations considers most of them.

Information presented in this document describe DCD’s design and Core verification methodology, and help our customers insure the quality of developed IP’s.

The Core verification process steps are always the same, and begins before the IP Code development. First of all, DCD’s engineers analyze in detail the available documentation, describing the function or algorithm to implement. After that there is prepared a detailed specification and implementation schedule. The internal architecture, and structure of all core modules is planned in details. Next, basing on the matter knowledge, there is prepared a tests plan, the test vectors are generated, and the structure of the test bench is planned.

IP design flow



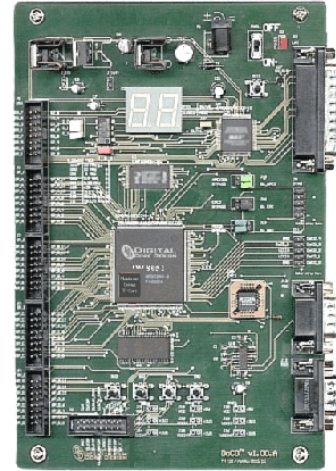
After completion of that strenuous conception work we are ready to **start developing** of the IP Core. Since the first line of code, DCD’s engineers lay a special attention to write the code conforming to the best software design practice and all commonly known design methodologies and rules, to maintain the best core quality and reusability. During a code development stage its compatibility with the specification is constantly verified using a previously generated test vectors, and any incompatibility is immediately analyzed and eliminated. The code coverage tools are used to determine whether the entire functionality of the module is being exercised. The code coverage tools check if all core code lines were reached, during simulation. Using of these tolls is very important, because only such method gives an objective measure of the test vectors validity.

The next step: the **code optimization** is performed after completion of code development. During this phase, our engineers optimize implemented algorithms, replace redundant logic, to meet best core performance and maintain smallest die size.

When we get satisfaction from the Core performance and a die size, we start checking code against the Naming Rules, Coding Style etc. and fulfill the OpenMORE

spreadsheet to get the OpenMORE rating. If any of the checking result doesn't meet DCD's internal quality regulations, the necessary modifications are done and the process is repeated.

When the Core Code development is finished, and it met all quality criteria, then we can start a **hardware verification** process. First of all the synthesis process is performed, and the timing netlist is generated, so we can do a post synthesis timing simulation, using a test bench and all possessed test vectors. The outputs from the core must match those from the silicon or the standard on a cycle-by-cycle simulation. Whatever hardware tool is used, the key verification technique is to compare the results from running the test vectors developed earlier against the physical target and against the core running in a simulator. These results must match.



After that the IP is ported to few FPGA technologies, and its functionality is checked with Vendors simulation tools. When all these verification stages are completed successfully we can start the final verification phase: **implementation in hardware** (FPGA devices) and running in a real application.

Successful completion of all design and verification steps, give the signal that Core is ready to release and we can be sure that the DCD's Core is as **risk free** as possible and fully compatible with a specification or an original part. Since DCD cooperate very closely with most programmable devices vendors, our cores functionality is checked and confirmed by third party organizations such as ALTERA-AMPP, XILINX-AllianceCORE or LATTICE-ispLeverCORE.



Our verification process is so precise and complex, that when the DCD's core is released we know we have achieved our goal of building the most **risk free** product possible. Purchasing of DCD's Intellectual Property can be best IP investment decision.