



DFPCOMP

Floating Point Comparator Unit

ver 2.07

OVERVIEW

The DFPCOMP compares two arguments. The input numbers format is according to IEEE-754 standard. DFPCOMP supports single precision real numbers. Compare operation was pipelined up to 1 level. Input data are fed every clock cycle. The first result appears after 1 clock period latency and next results are available **each clock** cycle. Full IEEE-754 unordered compare function is included.

APPLICATION

- Math coprocessors
- DSP algorithms
- Embedded arithmetic coprocessor
- Data processing & control

KEY FEATURES

- Full IEEE-754 compliance
- Single precision real format support
- Simple interface
- No programming required
- 1 level pipeline
- Results available at every clock
- Fully configurable
- Fully synthesizable, static synchronous design with no internal tri-states

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, One Year licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

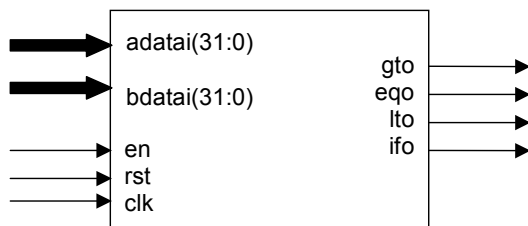
All trademarks mentioned in this document are trademarks of their respective owners.

<http://www.DigitalCoreDesign.com>
<http://www.dcd.pl>

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except One Year license where time of use is limited to 12 months.

- Single Design license for
 - VHDL, Verilog source code called HDL Source
 - Encrypted, or plain text EDIF called Netlist
- One Year license for
 - Encrypted Netlist only
- Unlimited Designs license for
 - HDL Source
 - Netlist
- Upgrade from
 - HDL Source to Netlist
 - Single Design to Unlimited Designs

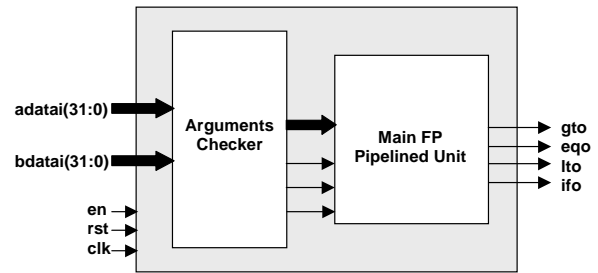
SYMBOL



PINS DESCRIPTION

| PIN | TYPE | DESCRIPTION |
|--------------|--------|---------------------|
| clk | Input | Global system clock |
| rst | Input | Global system reset |
| en | Input | Enable computing |
| adatai[31:0] | Input | A data bus input |
| bdatai[31:0] | Input | B data bus input |
| gto | output | A>B output |
| eqo | output | A=B output |
| lto | output | A<B output |
| ifo | output | Invalid results |

BLOCK DIAGRAM



Arguments Checker - performs input data analyze against IEEE-754 number standard compliance. The appropriate numbers and information about the input data classes are given as the results to Main FP Pipelined Unit.

Main FP Pipelined Unit - performs floating point compare function. Gives the complex information about the results and makes final flags settings.

CONTACTS

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check <http://www.dcd.pl/apartn.php>