



DFPSQRT

Floating Point Pipelined Square Root Unit ver 2.07

OVERVIEW

The DFPSQRT uses the **pipelined** mathematics algorithm to compute square root function. The input number format is according to IEEE-754 standard. DFPSQRT supports single precision real numbers. SQRT operation can be pipelined up to 9 levels. Input data are fed every clock cycle. The first result appears after 9 clock periods latency and next results are available **each clock** cycle. Precision and accuracy are parameterized.

APPLICATION

- Math coprocessors
- DSP algorithms
- Embedded arithmetic coprocessor
- Data processing & control

KEY FEATURES

- Full IEEE-754 compliance
- Single precision real format support
- Simple interface
- No programming required
- 9 levels pipelining
- 24-bit accuracy, 6 fractional decimal digits
- Results available at every clock
- Fully configurable

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- ◆ Fully synthesizable, static synchronous design with no internal tri-states

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

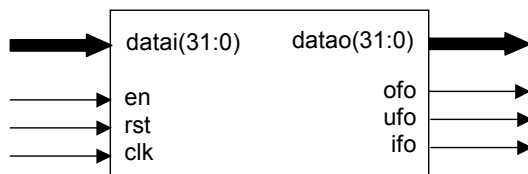
<http://www.DigitalCoreDesign.com>
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Unlimited Designs, One Year licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except One Year license where time of use is limited to 12 months.

- Single Design license for
 - VHDL, Verilog source code called HDL Source
 - Encrypted, or plain text EDIF called Netlist
- One Year license for
 - Encrypted Netlist only
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 - HDL Source
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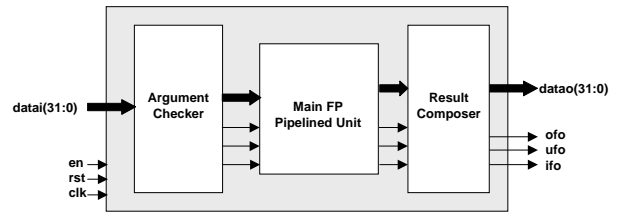
SYMBOL



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	Input	Global system clock
rst	Input	Global system reset
en	Input	Enable computing
datai[31:0]	Input	Data bus input
datao[31:0]	Output	Data bus output
ofo	Output	Overflow flag
ufo	Output	Underflow flag
ifo	Output	Invalid flag

BLOCK DIAGRAM



Arguments Checker - performs input data analyze against IEEE-754 number standard compliance. The appropriate numbers and information about the input data classes are given as the results to Main FP Pipelined Unit.

Main FP Pipelined Unit - performs floating point square root function. Gives the complex information about the results to Result Composer module.

Result Composer - performs result rounding function, data alignment to IEEE-754 standard, and the final flags setting.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ASIC devices (all key features have been included):

Device	Optimization	Gates	F _{max}
0.25u typical	area	2950	100 MHz
	speed	6900	220 MHz
0.18u typical	area	2900	150 MHz
	speed	6150	350 MHz

Core performance in ASIC devices

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