

D6802

8-bit Microprocessor ver 1.01

OVERVIEW

Document contains brief description of D6802 core functionality. The D6802 is a 8-bit MCU IP Core. D6802 soft core is binary-compatible with the industry standard MC6802 8-bit microprocessor.

Two software-controlled power-saving modes, WAIT and HALT, are available to conserve additional power. These modes make the D6802 IP Core especially attractive for automotive and battery-driven applications.

D6802 is **fully customizable**, which means it is delivered in the exact configuration to meet users requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- Cycle compatible with original implementation
- Software compatible with industry standard MC6802
- Up to 256 bytes of Data Memory
- De-multiplexed Address/Data Bus to allow easy connection to memory
- Two power saving modes: HALT, WAI
- No internal reset generator or gated clock
- Scan test ready
- Technology independent HDL source code
- Core can be fully customized
- DoCD™- Hardware on Chip Debugger

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DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF
- ◆ VHDL & VERILOG test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

<http://www.DigitalCoreDesign.com>
<http://www.dcd.pl>

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- ◇ VHDL, Verilog RTL synthesizable source code called HDL Source
- ◇ FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

DESIGN FEATURES

- ◆ One global system clock
- ◆ Synchronous reset
- ◆ All asynchronous input signals are synchronized before internal use

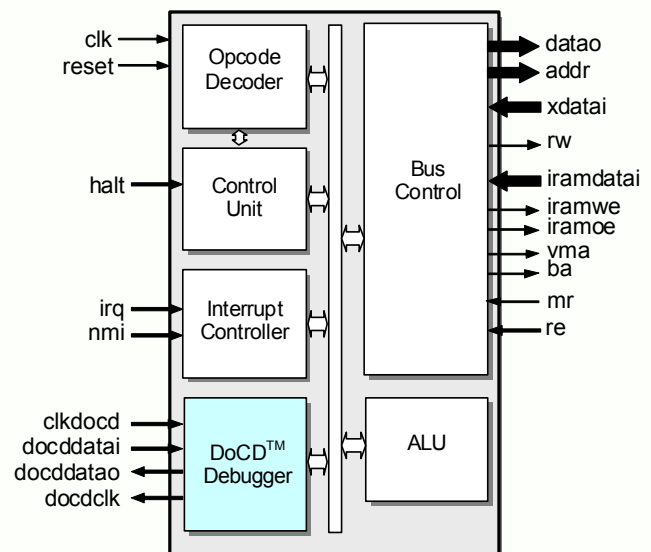
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global system clock
reset	input	Reset input
halt	input	Halt clock system
xdatai	input	External memory bus input
iramdatai	input	Internal RAM bus input
irq	input	Interrupt input
nmi	input	Non-maskable interrupt
re	input	Internal RAM enable input
mr	input	Memory ready input
addr	output	Common address bus
datao	output	Data bus output
rw	output	External RAM read/write
iramoe	output	Internal RAM OE
iramwe	output	Internal RAM WE
vma	output	Valid memory address
ba	output	Bus available output

clkdocd	input	Separate DoCD™ clock
docddatai	input	DoCD™ Serial Data input
docddatao	output	DoCD™ Serial Data Output
docdclk	output	DoCD™ Serial Clock Output

BLOCK DIAGRAM

Control Unit - Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages HALT input pin events.



Opcode Decoder - Performs an instruction opcode decoding and the control functions for all other blocks.

ALU - Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index register X and related logic like arithmetic unit, logic unit, multiplier and divider.

Bus Controller – Program Memory, Data Memory interface controls access into the program and data memories. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic.

Interrupt Controller - The interrupt requests may come from external pins (IRQ and NMI) as well as from particular peripherals.

DoCD™ - Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides

non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories,. Hardware breakpoints can be set and controlled on program memory, internal and external data memories. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern.

The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

PROCESSOR FAMILY OVERVIEW

The main features of each D68HCXX and DF68XX family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Speed acceleration	Physical Linear memory space	Paged Data Memory space	Motorola Memory Expansion Logic	Interrupt sources	Interrupt levels	Real Time Interrupt	Data Pointers	READY for Prg. And Data memories	Compare/Capture	Main Timer System	SCI (UART)	I/O Ports	SPI M/S Interface	Watchdog Timer	Pulse accumulator	Interface for additional SFRs	DoCD Debugger	Size – ASIC gates
D6802	1	64k	64k	-	2	2	-	-	-	-	-	-	-	-	-	-	-	✓	3 900
D6803	1	64k	64k	-	2	2	-	-	-	-	-	-	-	-	-	-	-	✓	6 000
D6809	1	64k	64k	-			-	-	-	-	-	-	-	-	-	-	-	✓	9 000

DF6805	4.1	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	6 700
D68HC05	1.0	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	6 700
DF6808	3.2	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	8 900
D68HC08	1.0	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	8 900

D68HC11E	1.0	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓	✓	✓	✓	✓	12 000
D68HC11F	1.0	64K	64K	-	20	17	✓	1*	*	5/3*	1*	✓*	7	✓	✓	✓	✓	✓	13 500
D68HC11KW1	1.0	1M	1M	✓	25	22	✓	1*	*	13/6*	3*	✓*	10	✓	✓	✓	✓	✓	21 000
D68HC11K	1.0	1M	1M	✓	20	17	✓	1*	*	5/3*	2*	✓*	7	✓	✓	✓	✓	✓	16 000
DF6811E	4.4	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	12 000
DF6811F	4.4	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	13 000
DF6811K	4.4	1M	1M	✓	20	17	✓	1*	*	5/3*	2*	✓*	7	✓	✓	✓	✓	✓	16 000

D68HCXX family of High Performance Microcontroller Cores

+ optional
* configurable

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CONTACT

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarter:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check <http://www.dcd.pl/apartn.php>