

D6803

8-bit Microcontroller ver 1.01

OVERVIEW

Document contains brief description of D6803 core functionality. The D6803 is an advanced 8-bit MCU IP Core with highly sophisticated, on-chip peripheral capabilities. The core in standard configuration has integrated on-chip major peripheral functions. An asynchronous serial communications interface (SCI) is included. The main 16-bit three programmable timers has three input capture and five output-compare lines.

Software-controlled power-saving mode, WAIT, is available to conserve additional power. This mode make the D6803 IP Core especially attractive for automotive and battery-driven applications.

The D6803 has built in real time hardware on chip debugger DoCD™, allowing easy software debugging and validation.

D6803 is **fully customizable**, which means it is delivered in the exact configuration to meet users' requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- Software compatible with industry standard 6803
- Cycle compatible with original implementation
- Power saving mode: WAIT
- Fully synthesizable, static synchronous design with no internal tri-states
- Scan test ready
- DoCD™- Hardware on Chip Debugger

DESIGN FEATURES

- ◆ One global system clock
- ◆ Synchronous reset
- ◆ All asynchronous input signals are synchronized before internal use

PERIPHERALS

The peripherals listed below are implemented in standard configuration of D6803.

- DoCD™ on Chip Debugger
 - Processor execution control
 - Read, write all processor contents
 - Hardware execution breakpoints
- Three 8-bit and one 5-bit I/O Ports
- Extended Interrupt Controller
- Main 16-bit timer/counter system
 - 16 bit free running counter
 - Compare/Capture functions
 - Timer clocked by internal source
- Full-duplex UART - SCI
 - Standard Non-return to Zero format (NRZ)
 - Integrated baud rate generator
 - Enhanced receiver data sampling technique
 - Overrun and Framing error detection
 - Wake-up block to recognize UART wake-up from IDLE condition
 - Three SCI related interrupts

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF
- ◆ VHDL & VERILOG test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- ◇ VHDL, Verilog RTL synthesizable source code called HDL Source
- ◇ FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

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PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global system clock
rst	input	Power on reset vector fetch
irq	input	Interrupt input
nmi	input	Non-maskable interrupt input
portxi	input	Port A,B,C, D inputs
rxid	input	SCI receiver data input
e	output	Clock bus synchronization
rw	output	Memory read/write output
as	output	Address strobe
portxo	output	Port A,B,C, D outputs
txid	output	SCI transmitter data output

clkdocd	input	DoCD™ clock input
docddatai	input	DoCD™ serial Data input
docddatao	output	DoCD™ Serial Data Output
docdclk	output	DoCD™ Serial Clock Output

BLOCK DIAGRAM

Control Unit - Performs the core synchronization and data flow control. This module manages execution of all instructions.

Opcode Decoder - Performs an instruction opcode decoding and the control functions for all other blocks.

ALU - Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index register X and related logic like arithmetic unit, logic unit, multiplier and divider.

Bus Controller – Program Memory, Data Memory interface controls access into the program and data memories. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic.

Interrupt Controller – Interrupt Control module is responsible for the interrupt manage sys-

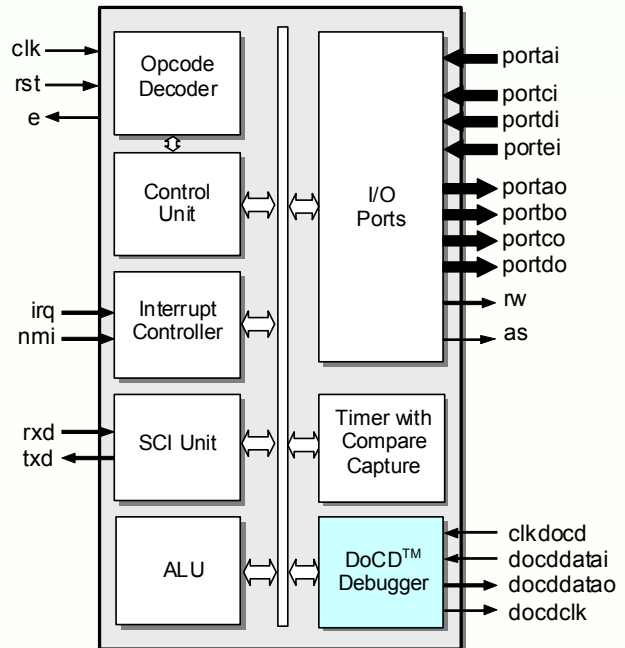
<http://www.DigitalCoreDesign.com>
<http://www.dcd.pl>

tem for the external & internal interrupts and exceptions processing. It manages auto-vectorized interrupt cycles, priority resolving and correct vector number creation.

Timer with Compare Capture - The programmable timer is based on free-running 16-bit counter, plus input capture/output compare circuitry. The timer can be used for many purposes including measuring pulse length of two input signals and generating two output signals. The timer has 16-bit architecture, hence each specific functional segment is represented by two 8-bit registers. These registers contains the high and low byte of that functional block. Accessing the low byte of a specific timer function allows full control of that function, however, an access of the high byte inhibits that specific timer function until the byte is also accessed. The input-capture channel has its own 16-bit time capture latch (input-capture register) and the output-compare channel has its own 16-bit compare register. Additional control bits permit software to control the edge(s) that trigger each input-capture function and the automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is essentially a software-oriented system. This structure is easily adaptable to a very wide range of applications although it is not as efficient as dedicated hardware for some specific timing applications.

SCI - The SCI is a full-duplex UART type asynchronous system, using standard non return to zero (NRZ) format : 1 start bit and a 1 stop bit. The Core resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore differences in baud rate between the sending device and the SCI are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time, and majority logic decides the sense for the bit. The receiver also has the ability to enter a temporary standby mode (called receiver wakeup) to ignore messages intended for a different receiver. Logic automatically wakes up the receiver in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole char-

acters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag.



I/O Ports - Three ports are 8-bit general-purpose bidirectional I/O system and one (PORTB) is 5-bit. The PORTA, PORTB, PORTC, PORTD data registers have their corresponding data direction registers DDRA, DDRB, DDRC, DDRD to control ports data flow. It assures that all D6803's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output then data registers are driven out of those pins. Reads from port pins configured as input causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins not configured as outputs do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.

DoCD™ - Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run,

step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

The separate CLKDOCD clock line allow the debugger to operate while the CPU is in STOP mode and the major clock line CLK is stopped.

OPTIONAL PERIPHERALS

There are also available an optional peripherals, not included in presented DF6808 Microcontroller Core. The optional peripherals, can be implemented in microcontroller core upon customer request.

- ADC Support
- Ethernet MAC Controller
- CAN, LIN Controllers
- I2C bus controller - Master
- I2C bus controller - Slave
- PWM – Pulse Width Modulation Timer
- Fixed-Point arithmetic coprocessor
- Floating-Point arithmetic coprocessor IEEE-754 standard single precision

MICROCONTROLLERS FAMILY OVERVIEW

The main features of each D68HCXX and DF68XX family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Speed acceleration	Physical Linear memory space	Paged Data Memory space	Motorola Memory Expansion Logic	Interrupt sources	Interrupt levels	Real Time Interrupt	Data Pointers	READY for Prg. And Data memories	Compare/Capture	Main Timer System	SCI (UART)	IO Ports	SPI M/S Interface	Watchdog Timer	Pulse accumulator	Interface for additional SFRs	DoCD Debugger	Size – ASIC gates	
D6802	1	64k	64k	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-	✓	3 900
D6803	1	64k	64k	-	2	2	-	-	-	-	-	-	-	-	-	-	-	-	✓	6 000
D6809	1	64k	64k	-			-	-	-	-	-	-	-	-	-	-	-	-	✓	9 000

DF6805	4.1	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	✓	6 700
D68HC05	1.0	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	✓	6 700
DF6808	3.2	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	✓	8 900
D68HC08	1.0	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	✓	8 900

D68HC11E	1.0	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓	✓	✓	✓	✓	✓	12 000
D68HC11F	1.0	64K	64K	-	20	17	✓	1*	*	5/3*	1*	✓*	7	✓	✓	✓	✓	✓	✓	13 500
D68HC11KW1	1.0	1M	1M	✓	25	22	✓	1*	*	13/6*	3*	✓*	10	✓	✓	✓	✓	✓	✓	21 000
D68HC11K	1.0	1M	1M	✓	20	17	✓	1*	*	5/3*	2*	✓*	7	✓	✓	✓	✓	✓	✓	16 000
DF6811E	4.4	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	✓	12 000
DF6811F	4.4	64k	64k	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	✓	13 000
DF6811K	4.4	1M	1M	✓	20	17	✓	1*	*	5/3*	2*	✓*	7	✓	✓	✓	✓	✓	✓	16 000

D68HCXX family of High Performance Microcontroller Cores

+ optional
* configurable

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