

DFPSQRT

Floating Point Pipelined Square Root Unit

v. 2.80

OVERVIEW

The DFPSQRT uses the **pipelined** mathematics algorithm, to compute square root function. The input number format conforms to IEEE-754 standard. DFPSQRT supports single precision real numbers. SQRT operation can be pipelined up to 9 levels. Input data are fed every clock cycle. The first result appears after 8 clock periods latency and next results are available **each clock** cycle. Precision and accuracy are parameterized.

APPLICATION

- Math coprocessors
- DSP algorithms
- Embedded arithmetic coprocessor
- Data processing & control

KEY FEATURES

- Full IEEE-754 compliance
- Single precision real format support
- Simple interface
- No programming required
- 8 levels pipelining
- 24-bit accuracy, 6 fractional decimal digits
- Results available at every clock
- Fully configurable

- Fully synthesizable, static synchronous design with no internal tri-states

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - FPGA netlist
- ◆ VHDL & VERILOG test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - NCSim automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

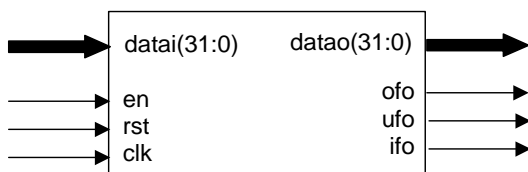
Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches. In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

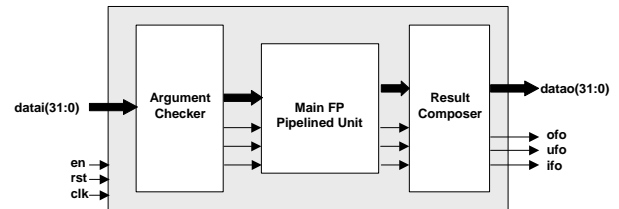
SYMBOL



PINS DESCRIPTION

| PIN | TYPE | DESCRIPTION |
|-------------|--------|---------------------|
| clk | Input | Global system clock |
| rst | Input | Global system reset |
| en | Input | Enable computing |
| datai[31:0] | Input | Data bus input |
| datao[31:0] | Output | Data bus output |
| ofo | Output | Overflow flag |
| ufo | Output | Underflow flag |
| ifo | Output | Invalid result flag |

BLOCK DIAGRAM



Arguments Checker - performs input data analysis against IEEE-754 number standard compliance. The appropriate numbers and information about the input data classes, are given as the results to Main FP Pipelined Unit.

Main FP Pipelined Unit - performs floating point square root function. Gives the complex information about the results, to Result Composer module.

Result Composer - performs result rounding function, data alignment to IEEE-754 standard, and the final flags setting.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ASIC devices :

| Device | Optimization | Gates | F _{max} |
|---------------|--------------|-------|------------------|
| 0.25u typical | area | 2950 | 100 MHz |
| | speed | 6900 | 220 MHz |
| 0.18u typical | area | 2900 | 150 MHz |
| | speed | 6150 | 350 MHz |

Core performance in ASIC devices



CONTACT

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