

D6840

Programmable Timer Module

ver 1.00

OVERVIEW

The D6840 is a programmable timer module compatible with 6840 industry standard. This IP core is designed for using as peripheral device for D68xx components or as separate module in applications where features of 6840 timer are useful. The D6840 has three separate 16-bit timers, with separate control and common status registers. The timers may be used for square wave generation with duty cycle regulation. Signal may be generated as continuous wave or single-shot mode. There is also capability for using D6840 module for frequency or pulse width measurement and comparison. The D6840 has interrupt which is useful in controlling module by CPU.

FEATURES

- Compatible with 6840 industry standard
- Three separate timers
- Two operation modes
 - *Wave synthesis*
 - *Wave measurement*
- Two generation modes
 - *Continuous*
 - *Single shot*
- Gating system for each clock input
- Separate timer outputs
- Prescaler mode for timer3 input clock
- External clock or E clock used for timer decrement
- Interrupt generation
- Split bus for input and output data

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- Fully synthesizable
- Synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

DESIGN FEATURES

The functionality of the D6840 core was based on MC6840. The following characteristics differentiate the D6840 from Texas Instruments devices:

- The IP core has additional clock input which is main clock domain. Main clock is at least four time faster than E clock. Typical, the main clock domain is the same as the clock for D68xx CPU which manages D6840 module.
- Input E is treated as input signal and synchronized to main clock domain. All counter events are related to E signal but are synchronized with main clock domain. Typical, the E signal is connected from D68xx CPU which manages D6840 module
- All latches implemented in original 6840 devices are replaced by equivalent flip-flop registers, with the same functionality

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - IP Core updates
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

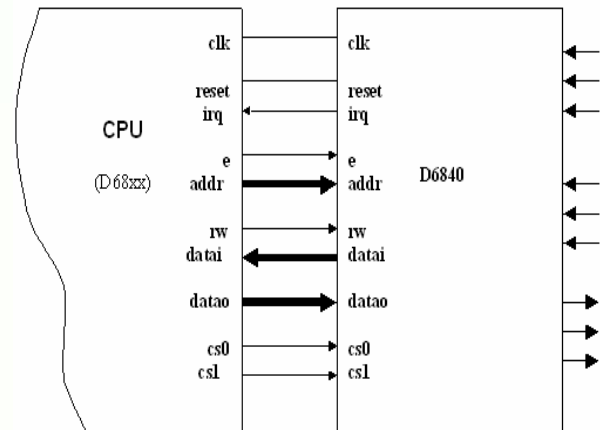
In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

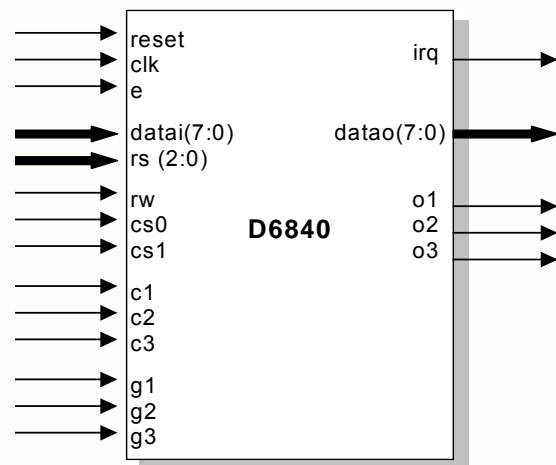
- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

APPLICATION

Typical D6840 and processor connection is shown in figure below.

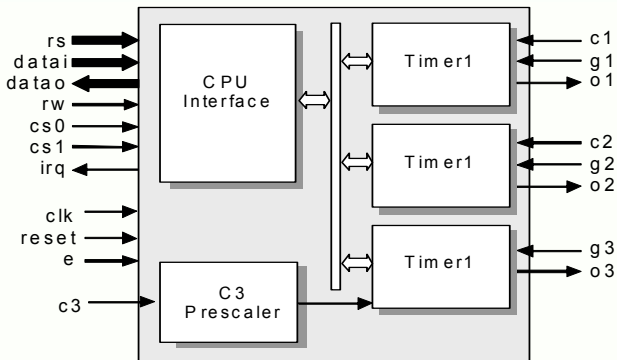


SYMBOL



BLOCK DIAGRAM

CPU Interface – Performs access to internal registers from CPU. This module contains all control and status registers. There is also MSB and LSB buffer used for access to 16-bit counter and Latch.



Timer1, 2, 3 – Main module, which contains 16-bit counter with all logic used for decrement, gating input clock and generating output signal and interrupt. **C3 Prescaler** – clock divider for C3 input. Used for divide clock by 8 in prescaled mode of timer3.

CONTACT

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PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Main clock
reset	input	Main reset
e	input	E clock
datai	input	Data bus input
rs	input	Register select
cs0	input	Chip select 0
cs1	input	Chip select 1
c1	input	Timer 1 external clock input
c2	input	Timer 2 external clock input
c3	input	Timer 3 external clock input
g1	input	Timer 1 clock gate input
g2	input	Timer 2 clock gate input
g3	input	Timer 3 clock gate input
irq	output	Interrupt request output
datao	output	Data bus output
o1	output	Timer 1 output
o2	output	Timer 2 output
o3	output	Timer 3 output