DFDCT

Forward Discrete Cosine Transform

ver 1.00

OVERVIEW

The Forward Discrete Cosine Transform (FDCT) is a transformation method that converts the block of input samples from spatial domain to its constituent frequency components as represented by a set of coefficients. For an image the FDCT is performed on 2-D array of samples, resulting in a 2-D array of frequency coefficients. The lower frequency coefficients appear toward the upper left-hand corner of the FDCT matrix, and the higher frequency coefficients are in the lower right-hand corner of the FDCT matrix.

The DFDCT core can perform Forward Discrete Cosine Transform on an 8x8 block of samples. The algorithm used for the calculation is based on the following equation:

$$Y_{uv} = \frac{2k(u)k(v)}{\sqrt{M \cdot N}} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} X_{mn} \cos\left[\frac{(2m+1)u\pi}{2M}\right] \cos\left[\frac{(2n+1)v\pi}{2N}\right]$$

where:

$M = N = 8$ are dimensions of DCT matrix

X_{mn} are the input image samples

Y_{uv} are the output coefficients

$k(u) = k(v) = \frac{1}{\sqrt{2}}$ for $u = v = 0$ and

$k(u) = k(v) = 1$ otherwise

The DFDCT core uses the row/column algorithm where transformation is implemented as two separate one dimensional (1-D) processes.

The DFDCT core implements 8-point 2D Forward Discrete Cosine Transform. The DFDCT is high performance and area optimized module designed for reuse in wide range of ASIC and FPGA technologies. It can be used in any multimedia and digital video applications.

KEY FEATURES

- 8x8 DCT block size
- Low latency (77 clock cycles)
- Continuous operation (one clock cycle per sample)
- Supports signed and unsigned input data format (zero-level shifting)
- Configuration parameters :
  - *Input data bus width*
  - *Output data bus width*
  - *Cosine coefficients width*
  - *Transpose memory bus width*
  - *Internal precision*
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

APPLICATIONS

- JPEG image compression standard
- MPEG1 digital video standard
- MPEG2 digital video standard
- MPEG4 digital video standard
- H.261 video conferencing standard
- H.263 video conferencing standard

http://www.DigitalCoreDesign.com
http://www.dcd.pl

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - FPGA netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

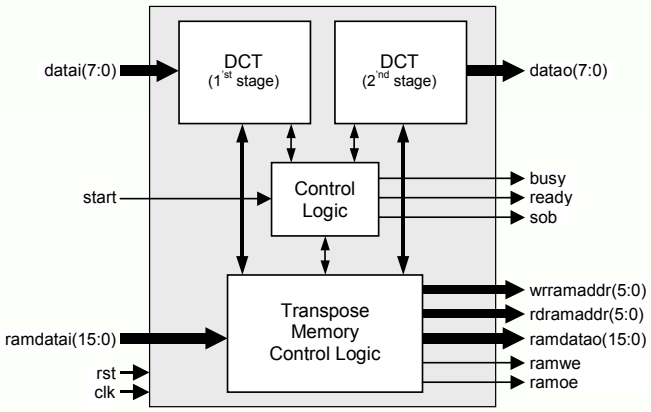
In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

BLOCK DIAGRAM

Figure below shows the DFDCT IP Core block diagram.



DCT (1'st stage) – This block performs 1-D Discrete Cosine Transform on row-wise input samples. Results of this computation stage are stored into the Transpose Memory. This processing stage comprises a set of multiply-accumulate units as well as Cosine lookup table for respective DCT computation.

DCT (2'st stage) – This block performs 1-D Discrete Cosine Transform on column-wise data stored in Transpose Memory by 1st stage. Results of this computation stage (DCT output coefficients) are available on the DATAO output bus. This processing stage comprises a set of multiply-accumulate units as well as Cosine lookup table for respective DCT computation.

Control Logic – Receives input control signal (START) and generates output control signals (BUSY, READY, SOB) as well as all internal control signals for both DCT stages and Transpose Memory Control Logic block. It synchronizes internal data flow.

Transpose Memory Control Logic – This module manages communication between both DCT stages and Transpose Memory. It generates all memory control signals (WRRAMADDR, RDRAMADDR, RAMWE, RAMOE) and is directly connected to Transpose Memory data buses (RAMDATAO, RAMDATAI).

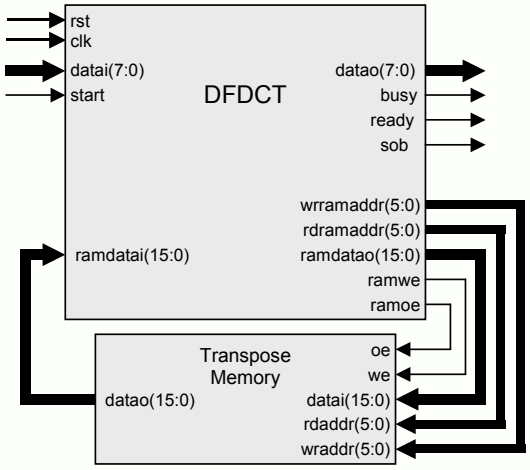
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock.
rst	input	Global reset.
datai(7:0)*	input	Data bus for DCT input samples.
start	input	Indicates that the first sample of the block is available for processing.
ramdatai(14:0)*	input	Data bus from transpose memory.
datao(10:0)*	output	Data bus for DCT output coefficients.
busy	output	Indicates that DCT core can process new block of data.
ready	output	Indicates that DCT output coefficients are available on datao bus.
sob	output	Start Of Block output. Signalizes that the first element (DC coefficient) of the output block is available on the datao bus.
ramdatao(14:0)*	output	Data bus for transpose memory.
wrramaddr(5:0)	output	Transpose memory write address.
rdramaddr(5:0)	output	Transpose memory read address.
ramwe	output	Transpose memory write enable.
ramoe	output	Transpose memory output enable.

* - All data buses are presented in this document with default width. The width can be changed by setting appropriate parameter in package file.

IMPLEMENTATION

Figures below show the typical DFDCT implementation.



DFDCT typical implementation

CONTACT

For any modification or special request, please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check http://www.dcd.pl/apartn.php