DSDRAM

Configurable SDRAM controller

ver 1.00

OVERVIEW

The DSDRAM is a soft Core of configurable SDRAM controller. It is fully compliant to the JEDEC PC100/133 standards. The DSDRAM can operate with any SDRAM memory device in terms of size, and required timing parameters. All access timing parameters such as CAS latency, refresh interval, etc., are programmable to support different speed grades of SDRAM devices and different operating frequencies. The timing parameters can be set to the proper default values during synthesis time.

It is very small, efficient, static fully synchronous design with no internal tri-state buffers and signals.

KEY FEATURES

- Supports any SDRAM discrete devices
- PC 66/100/133 SDRAM
- SDRAM from 16 Mbit to 1024 Mbit sizes
- Programmable data size
  - *8, 16, and 32 bits*
- Supports all burst lengths
  - *1, 2, 4, 8 and full page*
- CAS latency
  - *1, 2, and 3*
- Programmable access timing parameters
- Supports multiple external SDRAM banks
- Automatic refresh generation with programmable refresh intervals
- Self refreshing mode
- Fully synthesizable, static design with no internal tri-states

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - IP Core updates
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

http://www.DigitalCoreDesign.com
http://www.dcd.pl

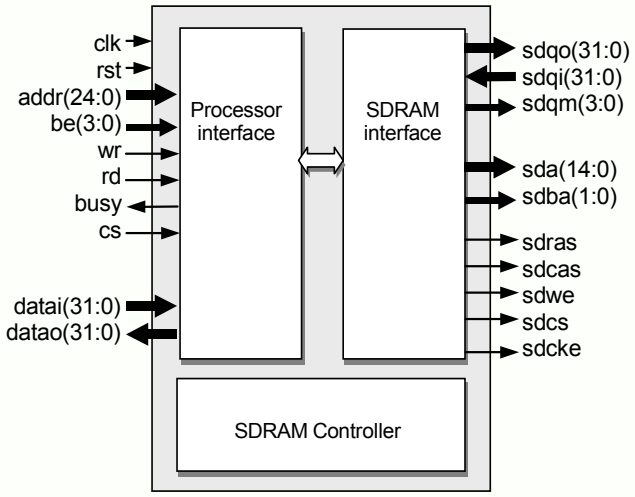
There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

BLOCK DIAGRAM

Processor Interface - unit managing communication between processor and internal SDRAM controller module. Control commands are issued to SDRAM interface based on state of read/write and chip select signals.

SDRAM Interface - unit translating internal states of SDRAM controller to SDRAM chip signal formats. It manages data flow between Processor Interface and SDRAM chip



SDRAM Controller - main unit responsible for proper control of SDRAM chip. It automatically issues refreshing commands to preserve valid data inside SDRAM chip. It also issues NOP, LOAD MODE REGISTER, READ, WRITE, (AUTO)PRECHARGE, ACTIVE commands.

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
datai(31:0)[1]	input	Processor data bus (input)
be(3:0)[3]	input	Processor byte enable
addr(24:0)[2]	input	Processor address bus
rd	input	Processor data read
wr	input	Processor data write
sdqi(31:0)[1]	output	SDRAM data bus (input)
datao(31:0)[1]	output	Processor data bus (output)
busy	output	Processor data busy indicator
sdqo(31:0)[1]	output	SDRAM data bus (output)
sdqm(3:0)[3]	output	SDRAM byte mask lines
sda(14:0)[4]	output	SDRAM address bus
sdba(1:0)[5]	output	SDRAM bank address lines
sdras	output	SDRAM RAS line
sdcas	output	SDRAM CAS line
sdwe	output	SDRAM write enable line
sdcs	output	SDRAM chip select line
sdcke	output	SDRAM clock enable line

Notes:

[1] - bus size is configurable as 8, 16, 32, 64 bits of wide

[2] - address size is automatically adjusted based on number of ROWS, COLUMNS, and BANKS of SDRAM chip (byte count)

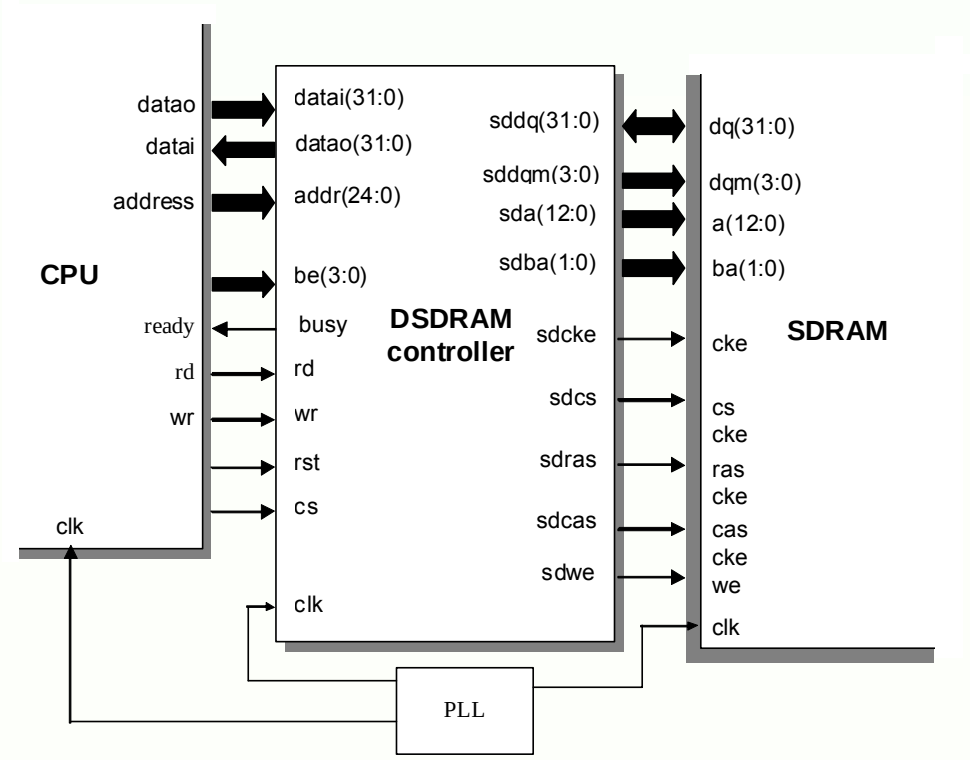
[3] - number of byte enable lines is automatically adjusted depend on data bus size and can have 1, 2, 4 or 8 lines

[4] - SDRAM address size depends on number of memory's ROWS

[5] - BANKS bus size is user configurable, and can have 1, or 2 bits

TYPICAL DSDRAM CONNECTION

Below is shown typical connection of DSDRAM Controller to microprocessor and SDRAM memory.



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