

# DoCD™

## PIC Cores - DCD on Chip Debug System

### v. 3.01

#### OVERVIEW

**DCD on Chip Debug System (DoCD™)** prominently cuts debugging time. Integrating DCD IP Cores with a Hardware Assisted Debugger and Debug IP Core, provides a powerful SoC development tool, with advanced features.

The DoCD™ system consists of three major blocks:

- Debug IP Core
- Hardware Assisted Debugger
- Debug Software



The Debug IP Core block is a **real-time hardware debugger**, which provides access to whole chip registers, memories and peripherals connected to DCD's IP Core (Dx8051/Dx80390/ DRPIC/DFPIC) and controls CPU work by **non-intrusive** method. A high-performance Hardware Assisted Debugger (**USB-DTAG**) is connected to the target system containing the DCD's core, either in FPGA or ASIC. The Hardware

Assisted Debugger manages communication between the Debug IP Core inside silicon, using DTAG protocol and Debug Software, using USB port.

#### SYSTEM FEATURES

An unlimited number of software breakpoints can be set anywhere in the physical address space of the processor (in Program Memory space, RAM and SFRs). If at least one software breakpoint is set, program is executed in automatic step by step mode, with checking, if certain breakpoint condition is met. Program execution is halted, when breakpoint condition is already met, and its execution can be resumed at any time in any appropriate mode.

- **HARDWARE BREAKPOINTS:**

The number of hardware breakpoints is limited to four in different address spaces. Like software breakpoints, hardware execution breakpoints can be set in Program Memory space, RAM and SFRs. Like their software counter-parts, they stop program execution just prior an instruction is being executed. The difference is in the method of program execution. In this case program is run with full clock speed (in real-time) and processor is halted, when hardware signals real breakpoint condition.

- **MIXED MODE BREAKPOINTS:**

Mixed breakpoint mode is also allowed and it means, that software and hardware breakpoints are mixed in the system. This gives you the flexibility in the debugging - for example, two dif-

ferent break conditions can be set at the same address space, by using software and hardware breakpoints. In each breakpoint mode, halt means: CPU is halted and instructions are no longer being fetched, all peripherals are running and are not affected by halt.

#### ● SCALED SOLUTION:

Due to the fact, that many SoC designs have both power and gate limitations, DCD provides a scaled solution. Debug extensions can be scaled to control gate counts. The benefit is fewer gates - for lower use of power and core size, while maintaining excellent debug abilities

#### ● HOST REQUIREMENTS:

A Pentium class computer with minimum 512 MB of memory, 32 MB of free space on Hard Disk, CD-ROM drive, USB port and Windows 2000/2003/XP/7 operating system, are required.

## DEBUG IP CORE

The Debug IP Core can be provided as VHDL or Verilog source code, as well as CPLD/FPGA EDIF netlist, depending on the customer requirements. Due to the fact, that many SoC designs have both power and area limitations, DoCD™ provides a scaled solution. Debug IP Core can be scaled to control gate count. The benefit is fewer gates - for lower use of power and core size, while maintaining excellent debug abilities. Typically, all of the features are utilized in pre-silicon debug (i.e. hardware emulation or FPGA evaluation) with less features availed in the final silicon.

## FEATURES

- ◆ Processor execution control
  - Run, Halt
  - Reset
  - Step into instruction
  - Skip Instruction
- ◆ Read-write all processor contents
  - Program Counter (PC)
  - Program Memory
  - Data Memory

- Special Function Registers (SFRs)
- Accumulator A, B
- Index registers X, Y
- Condition Code Register - CCREG
- Stack Pointer
- ◆ Unlimited number of software breakpoints
- Program Memory
- Data Memory
- Special Function Registers (SFRs)
- ◆ Hardware execution breakpoints
- Program Memory
- Data Memory
- Special Function Registers (SFRs)
- ◆ Hardware breakpoints activated at a
  - certain program address (PC)
  - certain address by any write into memory
  - certain address by any read from memory
  - certain address by write into memory a required data
  - certain address by read from memory a required data
- ◆ Automatic adjustment of debug data transfer speed rate between HAD and Silicon
- ◆ Three-wire communication interface
- ◆ Fully static synchronous design with no internal tri-states

## HAD

Hardware Assisted Debugger (HAD) is a hardware adapter, that manages communication between the Debug IP Core inside silicon and a USB port of the host PC running DoCD™ Debug Software.

## FEATURES

- ◆ USB communication interface to target host at FULL speed
- ◆ Synchronous communication interface to Debug IP Core through DTAG interface
- ◆ Supports following I/O voltage standards
  - 3.3 Volt systems
  - 2.5 Volt systems
  - 1.8 Volt systems
  - 1.5 Volt systems
- ◆ Single power supply directly from USB

- ◆ Small physical dimensions

## DEBUG SOFTWARE

The **DoCD™** Software (DS), is a Windows based application. It is fully compatible with nearly all existing PIC C compilers and Assemblers. The DS was designed to work in two major modes: software simulator mode and hardware emulator mode. Those two modes, allow the pre-silicon software validation in simulation mode and then, real-time debugging of developed software inside silicon - using emulator mode. Once loaded, the program may be observed in Source Window, run at full-speed, single stepped by machine or ASM-level instructions or stopped at any of the breakpoints.

The **DoCD™** Debug Software supports all DCD's PIC Cores (DRPIC16XXX, DFPIC16XXX) in the following architectures and particular configurations:

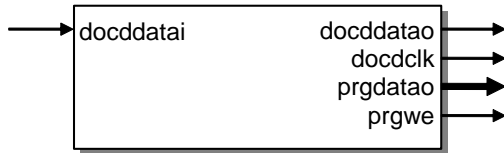
## FEATURES

- ◆ Two working modes
  - *hardware emulator*
  - *software simulator*
- ◆ Source Level Debugging:
  - *C level hardware/software breakpoints*
  - *C line execution*
    - *line by line*
    - *over function*
    - *out of function*
    - *skip line*
  - *ASM code execution*
    - *Instruction by instruction*
    - *over instruction*
    - *out of function*
    - *skip instruction*
  - *ASM and C source code view*
- ◆ Symbol Explorer provides hierarchical tree view of all symbols:
  - *modules*
  - *functions*
  - *blocks*
  - *variables*

- ◆ Symbolic debug including:
  - *variables*
  - *variable type*
- ◆ Contents sensitive Watch window
- ◆ Symbolic debug including:
  - *variables*
  - *variable type*
- ◆ Contents sensitive Watch window
- ◆ Unlimited number of software breakpoints
  - *Program Memory*
  - *Internal (direct) Data Memory (DM)*
  - *Special Function Registers (SFR)*
- ◆ Real-time hardware breakpoints
  - *Program Memory*
  - *Data Memory (DM)*
  - *Special Function Registers (SFR)*
- ◆ Set/clear software or hardware breakpoints in Assembler and C Source Code
- ◆ Load Program Memory content from:
  - *Intel HEX files*
  - *OMF object files*
  - *COD object files*
- ◆ Auto refresh of all windows
  - *Registers' W, FSR, STATUS, Stack Pointer and Hardware Stack, SFR registers*
  - *Data Memory (DM)*
  - *Special Function Registers (SFR)*
  - *Timers / Counters*
  - *Compare / Capture Channels*
  - *USART*
  - *I/O Ports*
- ◆ Dedicated windows for peripherals
- ◆ Configurable auto refresh time period with 1s step resolution
- ◆ Status bar containing number of actually executed instructions, number of clock periods and real processor speed rate
- ◆ The system runs on a Windows® 95/98/NT/2000/XP PC

## PINOUT

The following pins are used by DoCD™ debug IP Core.



PIN	TYPE	DESCRIPTION
docddatai	input	DoCD™ data input
docddatao	output	DoCD™ data output
docdclk	output	DoCD™ clock line
prgdatao	output	Program Memory output Bus
prgwe	output	Program Memory write enable

## AREA UTILIZATION

The following table gives a survey about the Debug IP Core area in the FPGA and ASIC devices.

Device vendor	Area
ALTERA	760 LC
XILINX	380 Slices
ASIC	2800 gates

## DFPIC&DRPIC FAMILY OVERVIEW

The family of DCD DFPICXX & DRPICXX IP Cores combine high-performance, low cost and small compact size, offering the best price/performance ratio in the IP Market. The DCD's Cores are dedicated for use in cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

DCD's DFPICXX & DRPICXX IP Cores family contains four 8-bit microcontroller Cores to meet your needs in the best way: DFPIC165X 12-bit program word, DFPIC1655X 14-bit program word, and DRPIC1655X and DRPIC166X single cycle microcontrollers, with 14-bit program word. All three microcontroller cores are binary compatible with widely accepted PIC16C5X and PIC16CXXX. They have a modified RISC architecture, two or four times faster than the original ones.

The DFPICXX & DRPICXX IP Cores are written in pure VHDL/VERILOG HDL languages, what makes them technologically independent. All of the DFPICXX & DRPICXX family members are supported by a power saving SLEEP mode, which allows you to configure the watchdog time-out period and a number of hardware stack levels. DFPICXX & DRPICXX can be fully customized according to your needs.

Design	Program Memory space	Program word length	Data Memory space	Number of instructions	I/O Ports	Timer 0	Timer 1	Timer 2	Watchdog Timer	CCP1	USART	Sleep Mode	External interrupts	Internal Interrupts	Wake up on port pin change	Speed rate	DoCD™ Debugger	Size (gate)
DFPIC165X	2k	12	128	33	24	✓	-	-	✓	-	-	✓	-	-	-	2	-	2 700
DFPIC1655X	64k	14	32k	35	16	✓	-	-	✓	-	-	✓	5	1	✓	2	✓*	3 900
DFPIC166X	64k	14	32k	35	32	✓	✓	✓	✓	✓	✓	✓	5	5	✓	2	✓*	6 000
DRPIC1655X	64k	14	32k	35	32	✓	-	-	✓	-	-	✓	5	1	✓	4	✓*	4 800
DRPIC166X	64k	14	32k	35	32	✓	✓	✓	✓	✓	✓	✓	5	5	✓	4	✓*	6 700

\* Optional

*DFPIC & DRPIC family of High Performance Microcontroller Cores*

## CONTACT

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