Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced micro-controllers and SoCs, we are designing solutions tailored to your needs.

The DCAN FD is a standalone controller for the Controller Area Network (CAN), widely used in automotive and industrial applications. It conforms to Bosch CAN 2.0B specification (2.0B Active) and CAN FD (flexible data-rate). The improved protocol overcomes standard CAN limits: data can be transmitted faster than with 1 Mbit/s and the payload (data field) is up to 64 byte long and limited to 8 byte anymore. When only one node is transmitting, the bit-rate can be increased, because no nodes need to be synchronized. Of course, before the transmission of the ACK slot bit, the nodes need to be re-synchronized. The core has a simple CPU interface (8/16/32 bit configurable data width), with small or big endianness addressing scheme. Hardware message filtering and 128 byte receive FIFO enable back-to-back message reception, with minimum CPU load. The DCAN FD is provided as HDL source code, allowing target use in FPGA or ASIC technologies.

**Features**
- Designed in accordance to ISO 11898-1:2015
- Supports CAN 2.0B and CAN FD frames
- Support up to 64 bytes data frames
- Flexible data rates supported
- 8/16/32-bit CPU slave interface with small or big endianness
- Simple interface allows easy connection to CPU
- Supports both standard (11-bit identifier) and extended (29 bit identifier) frames
- Data rate up to 8 Mbps
- Hardware message filtering (dual/single filter)
- 128 byte receive FIFO and transmit buffer
- Overload frame is generated on FIFO overflow
- Normal & Listen Only Mode
- Transceiver Delay Compensation up to three data bit long
- Single Shot transmission
- Ability to abort transmission
- Readable error counters
- Last Error Code
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

**Deliverables**
- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - FPGA Netlist
- VHDL /VERILOG test bench environment
  - Active-VERILOG automatic simulation macros
  - NCSim automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
  - Delivery of the IP Core and documentation updates, minor and major versions changes
  - Phone & email support

**Licensing**
Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.
Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.
There are two formats of the delivered IP Core:
- VHDL or Verilog RTL synthesizable HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM Netlist

**Block Diagram**

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**PIN OUT**

1 – configured data bus - 8-, 16- or 32
2 – byte enable (be) size is set accordingly to data bus size

**UNITs SUMMARY**

**Interface Management Logic (IML)** – interprets commands from the CPU, provides interrupt and status indication.

**Bit Stream Processor (BSP)** – translates messages into frames and vice versa.

**Baud Rate Prescaler (BRP)** – defines the length of time quantum.

**Bit Timing Logic (BTL)** – processes the bit time, calculates position of the sample point and performs synchronization.

**Error Management Logic (EML)** – is responsible for fault confinement handling.

**Acceptance Filter (ACF)** – decides, whether incoming messages are accepted or not, based on filter registers settings.

**TX/RX RAM interfaces** – interfaces to external dual port memories used by the DCAN core, to store received and transmitted frames.

**DSPI** allows direct interface to almost any existing synchronous serial peripheral.

**Performance**

The following table gives a survey about the Core area and performance in XILINX® devices after Place & Route:

<table>
<thead>
<tr>
<th>Device</th>
<th>Speed grade</th>
<th>FF</th>
<th>LUT</th>
<th>Memory bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>KINTEX 7</td>
<td>-3</td>
<td>476</td>
<td>1052</td>
<td>40</td>
</tr>
<tr>
<td>ARTIX 7</td>
<td>-3</td>
<td>476</td>
<td>1047</td>
<td>40</td>
</tr>
</tbody>
</table>

Core performance in XILINX® devices without CAN FD option

<table>
<thead>
<tr>
<th>Device</th>
<th>Speed grade</th>
<th>FF</th>
<th>LUT</th>
<th>Memory bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>KINTEX 7</td>
<td>-3</td>
<td>758</td>
<td>1655</td>
<td>256</td>
</tr>
<tr>
<td>ARTIX 7</td>
<td>-3</td>
<td>760</td>
<td>1696</td>
<td>256</td>
</tr>
</tbody>
</table>

Core performance in XILINX® devices with CAN FD option

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